Nanometer-scale III-V 3D MOSFETs

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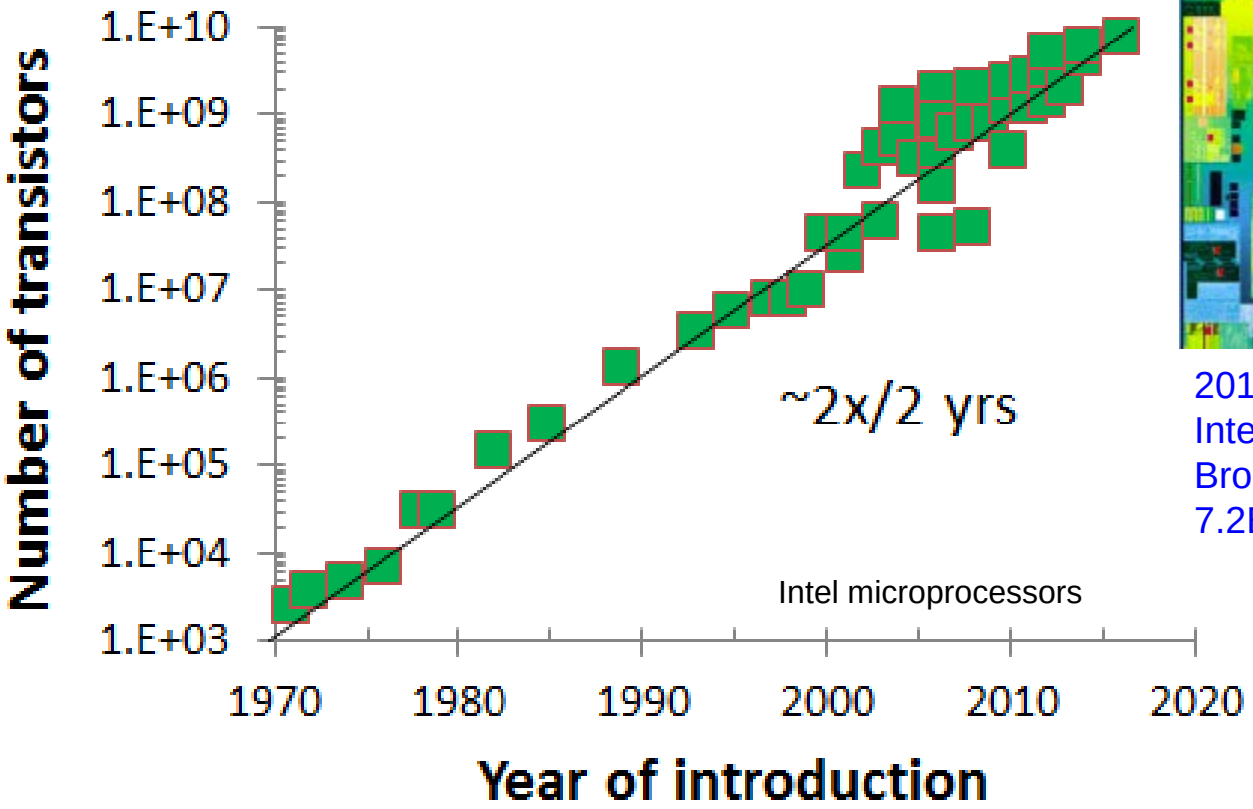
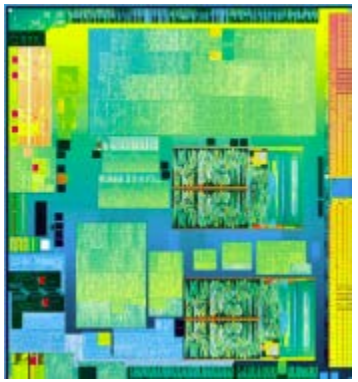
- Labs at MIT: MTL, EBL

Moore's Law

Moore's Law = exponential increase in transistor density

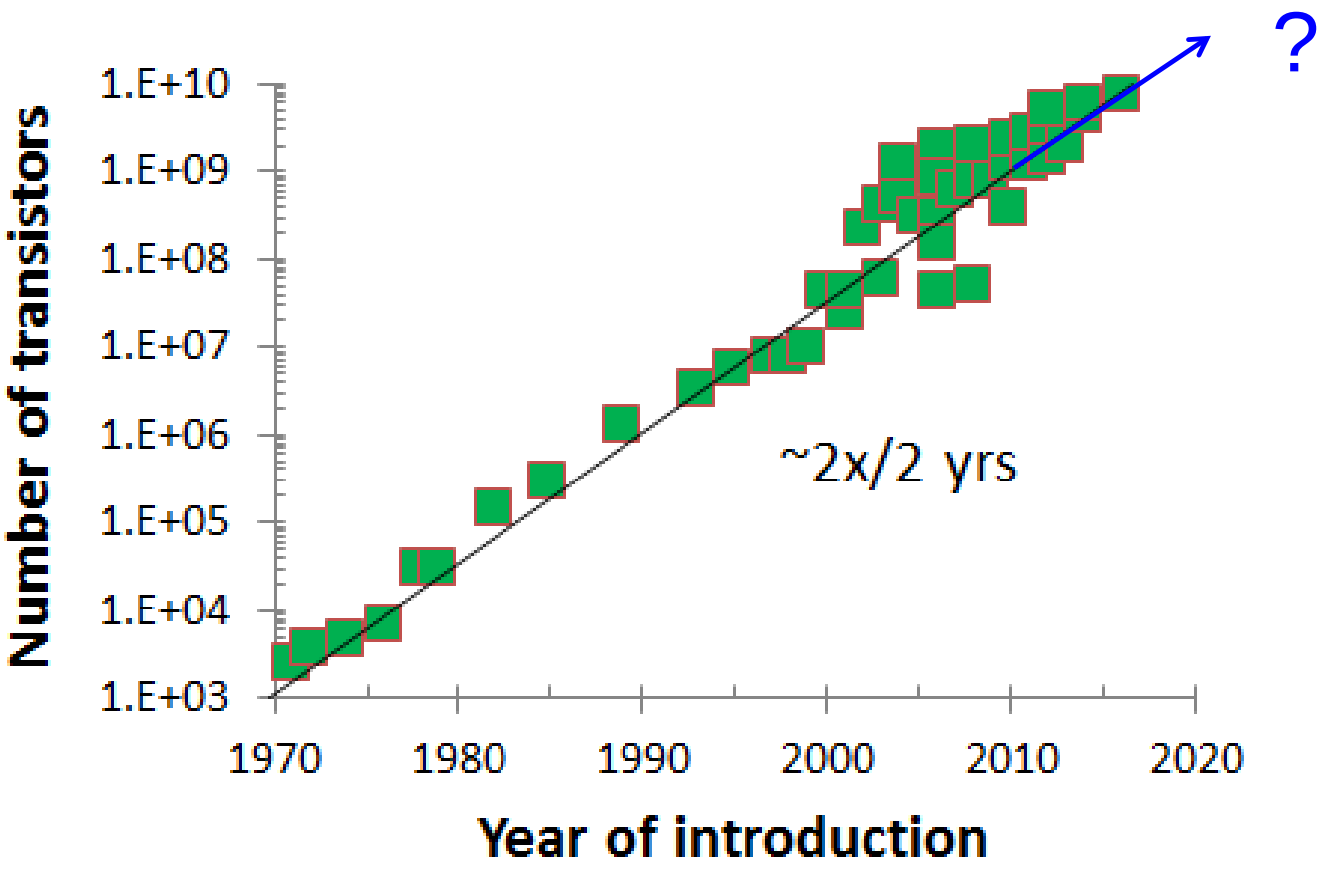




2016:
Intel 22-core Xeon
Broadwell-E5
7.2B transistors

Moore's Law

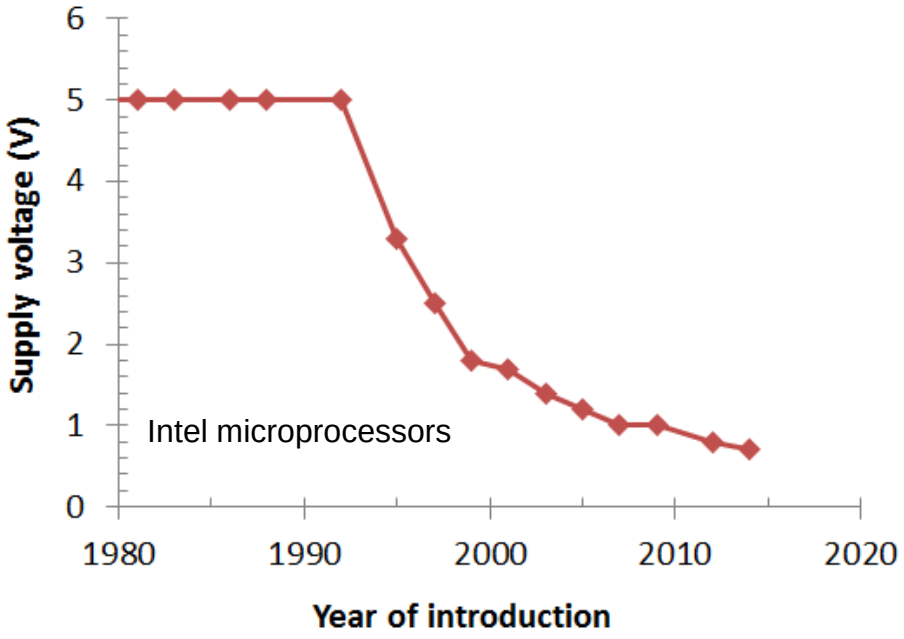
How far can Si support Moore's Law?



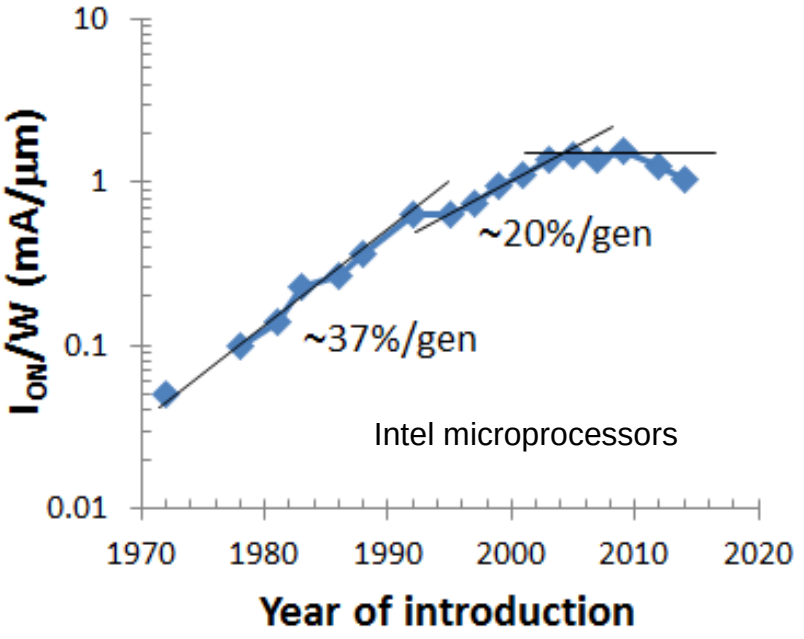
The problem:

Transistor scaling → Voltage scaling → Performance suffers

Supply voltage:



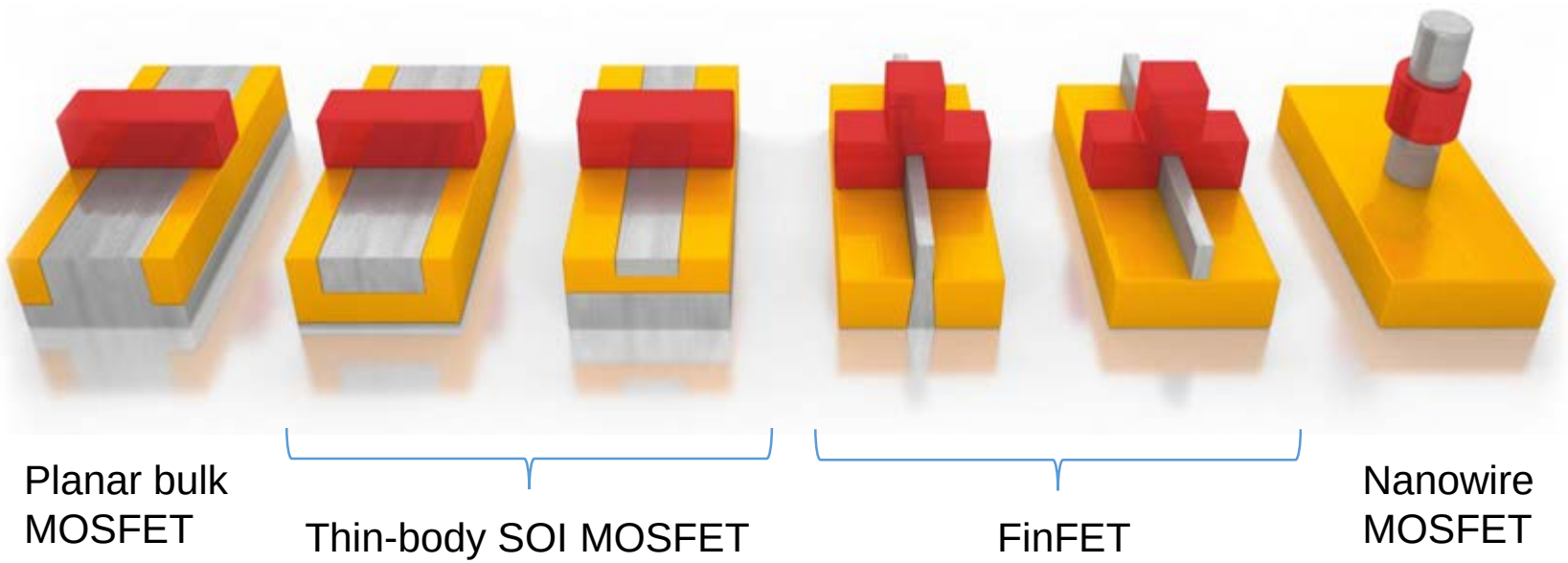
Transistor current density:



What can we do about this?

Moore's Law: it's all about MOSFET scaling

1. New device structures with improved scalability:



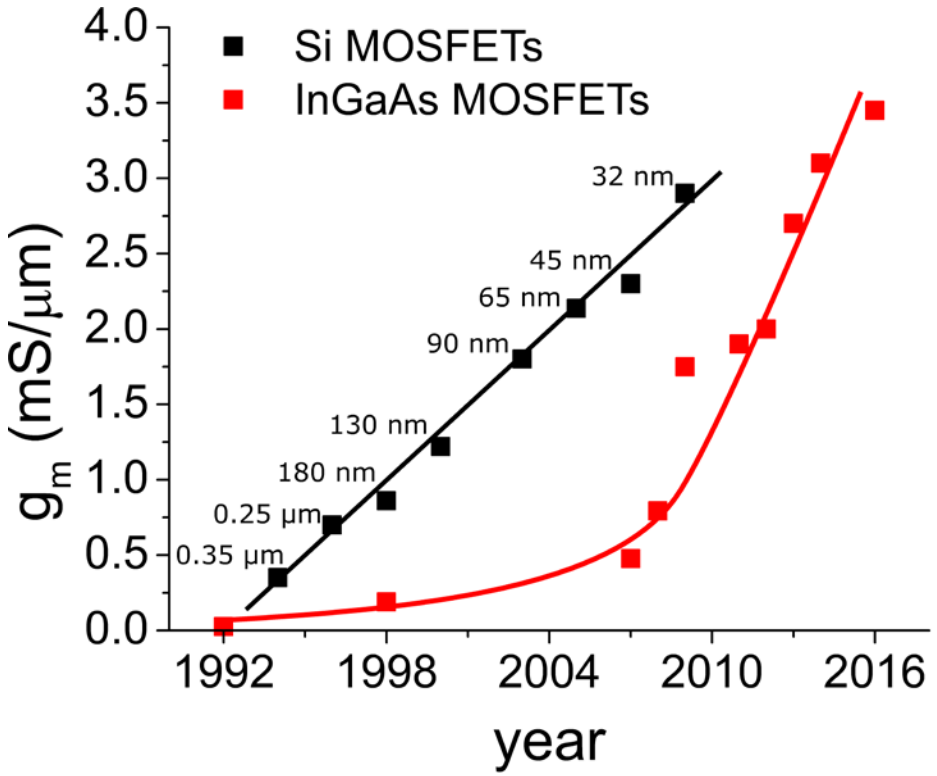
2. New materials with improved transport characteristics:

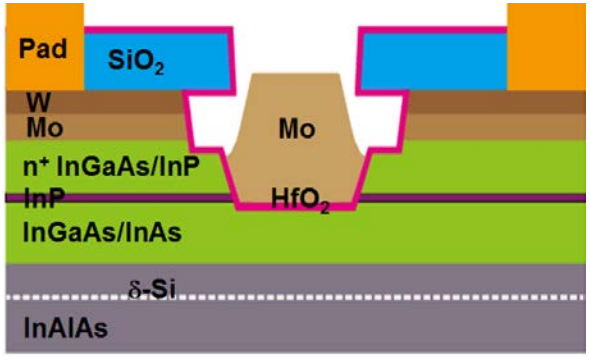
n-channel: Si → Strained Si → SiGe → InGaAs

p-channel: Si → Strained Si → SiGe → Ge → InGaSb

Planar Si and InGaAs MOSFET Benchmark

n-MOSFETs in Intel's nodes at nominal voltage

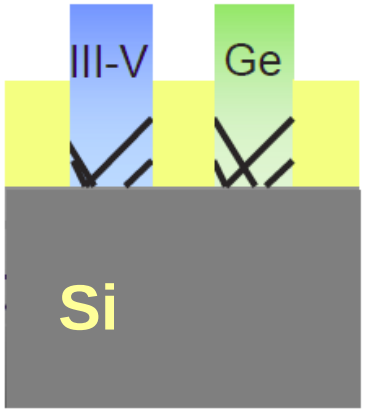




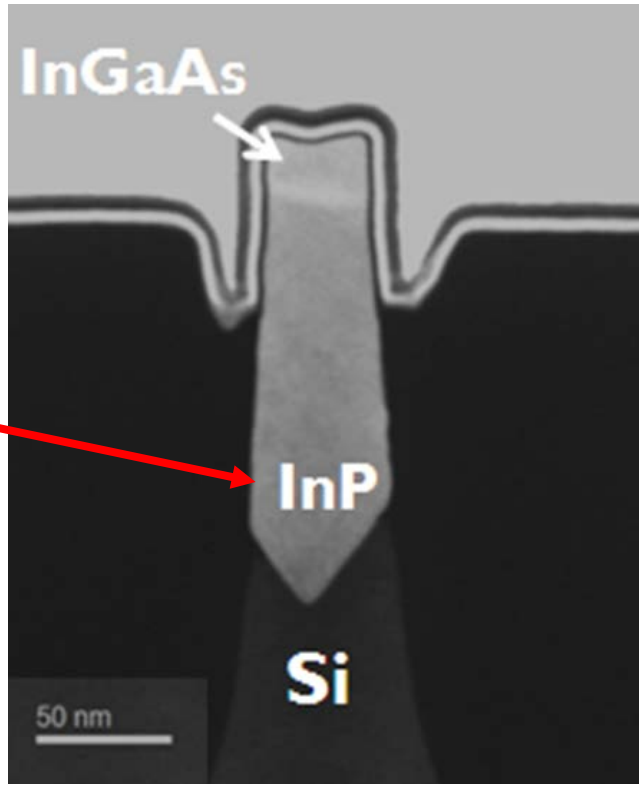
Comparisons always fraught with danger…

- Recent rapid progress thanks to ALD gate oxide
- Performance exceeds Si

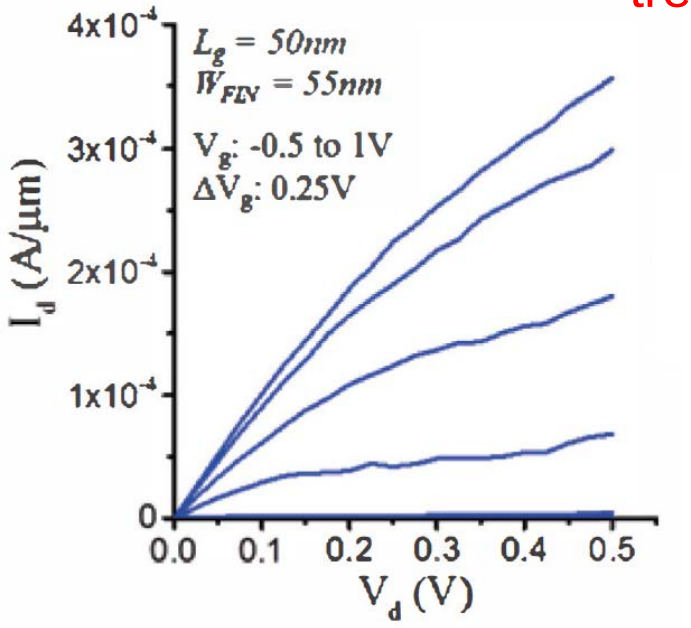
Bottom-up InGaAs FinFETs



Aspect-Ratio Trapping
Fiorenza, ECST 2010



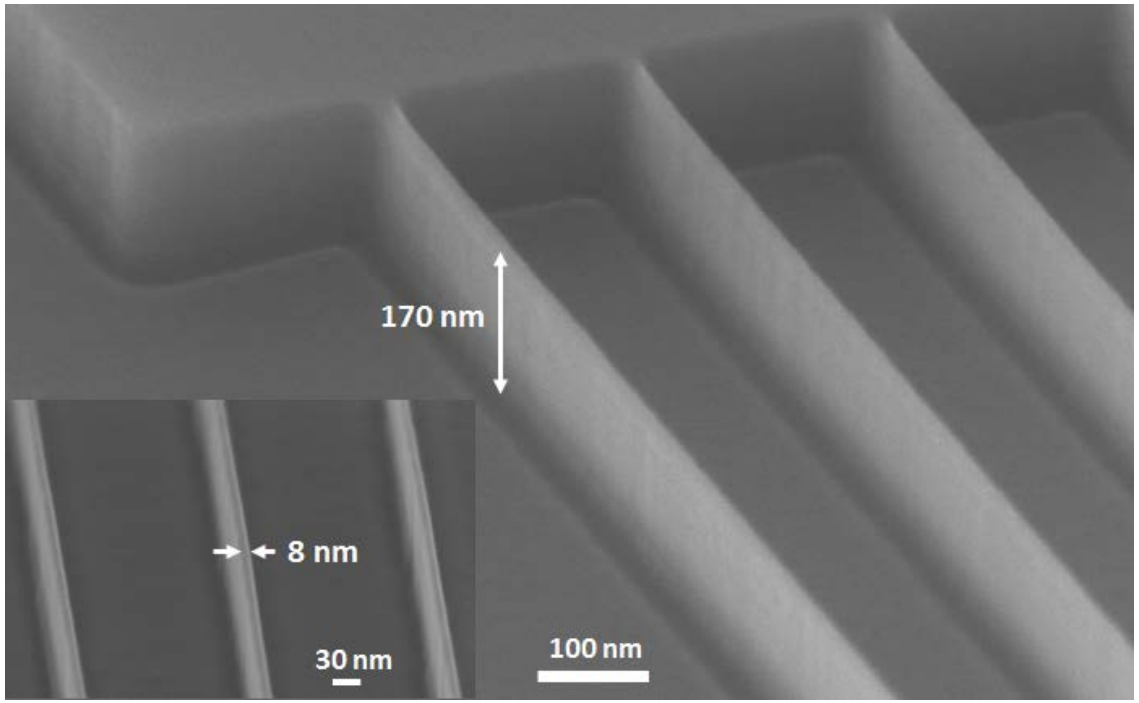
Epi-grown fin inside trench



Waldron, VLSI Tech 2014

InGaAs FinFETs @ MIT

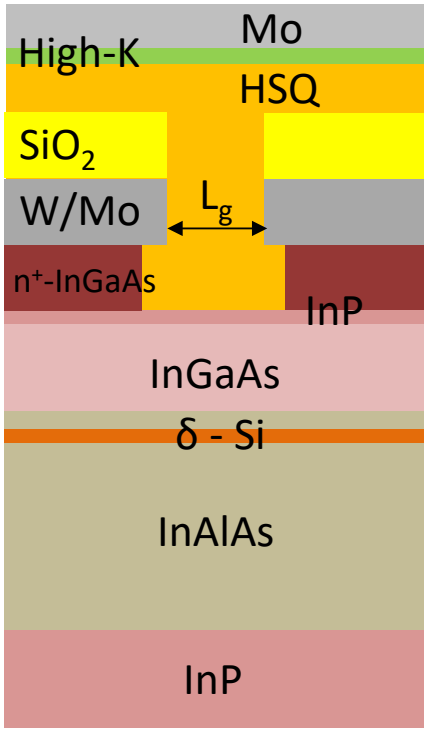
Key enabling technologies: $BCl_3/SiCl_4/Ar$ RIE + digital etch

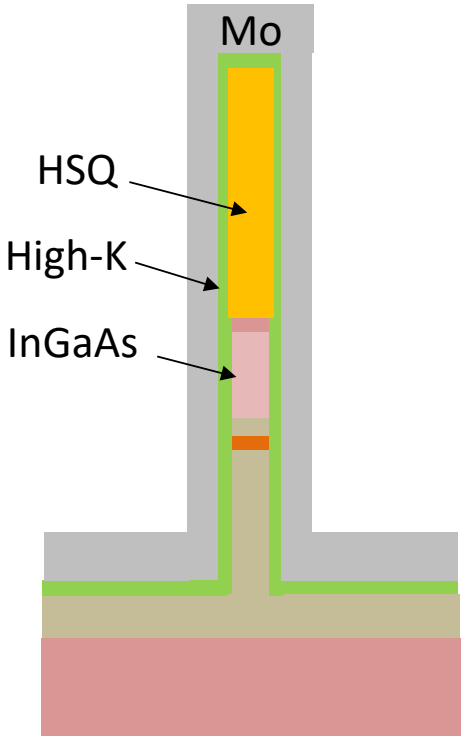


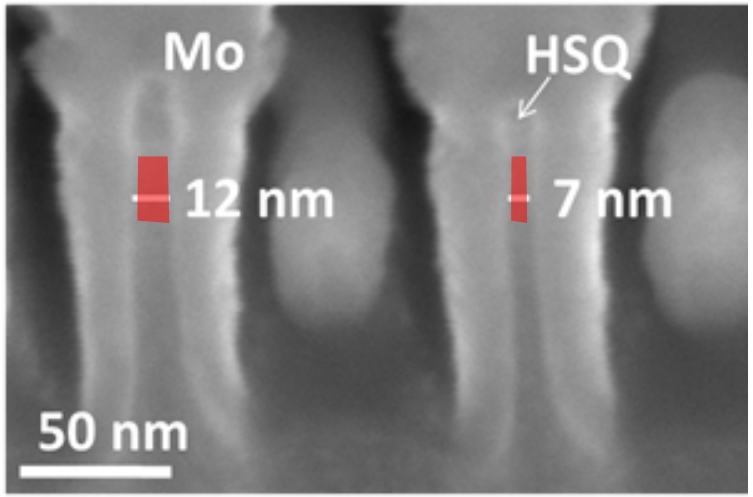
- Sub-10 nm fin width
- Aspect ratio > 20
- Vertical sidewalls

Vardi,
DRC 2014,
EDL 2015,
IEDM 2015

InGaAs FinFETs @ MIT





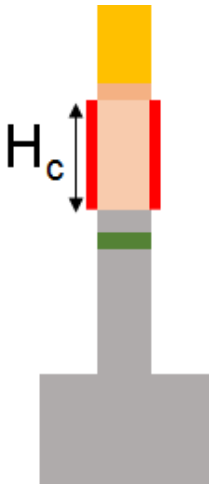


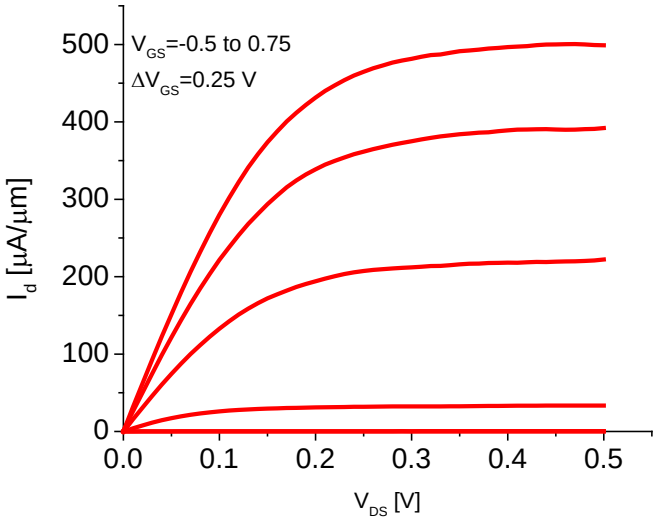
Vardi, VLSI Tech 2016
Vardi, EDL 2016

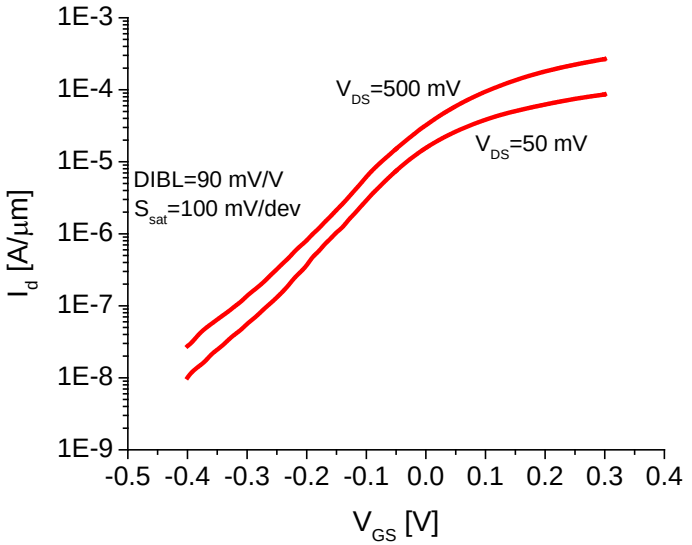
- Si-compatible process
- Contact-first, gate-last process
- Fin etch mask left in place → double-gate MOSFET

Most aggressively scaled FinFET

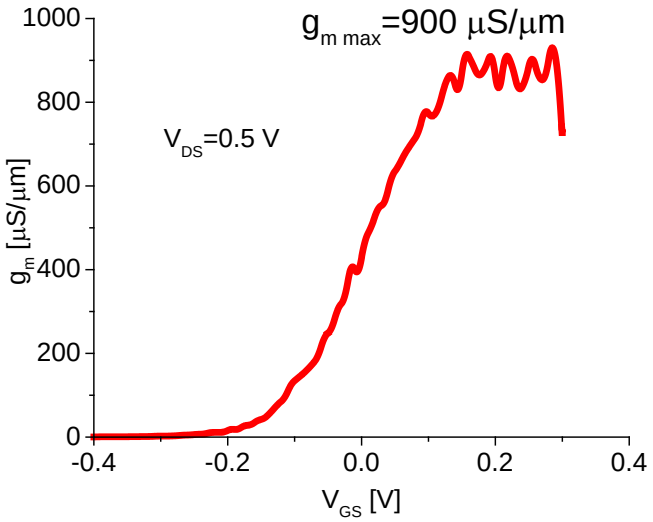
W_f=7 nm, L_g=30 nm, H_c=40 nm (AR=5.7), EOT=0.6 nm:







Current normalized by 2xH_c



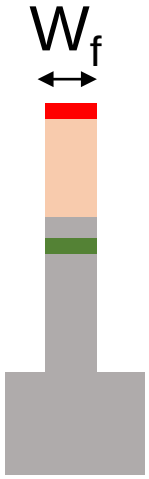
At V_{DS}=0.5 V:

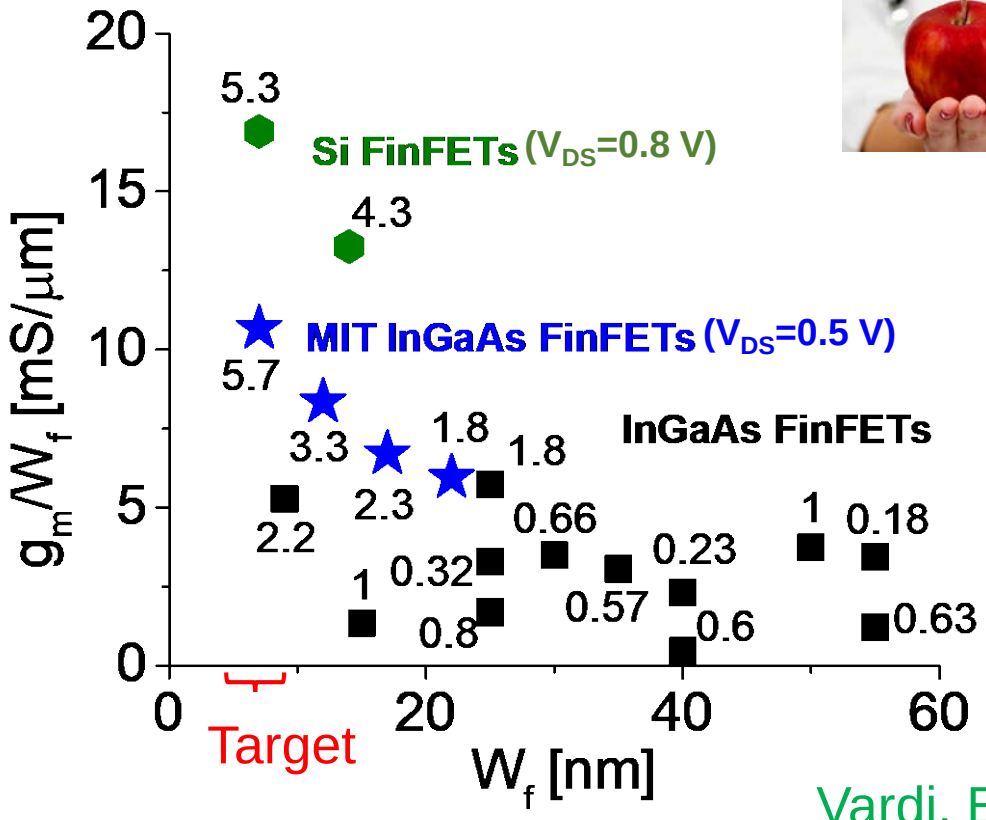
- g_m=900 μS/μm
- R_{on}=320 Ω.μm
- S_{sat}=100 mV/dec

Vardi, EDL 2016

InGaAs FinFET benchmarking

g_m normalized by fin width

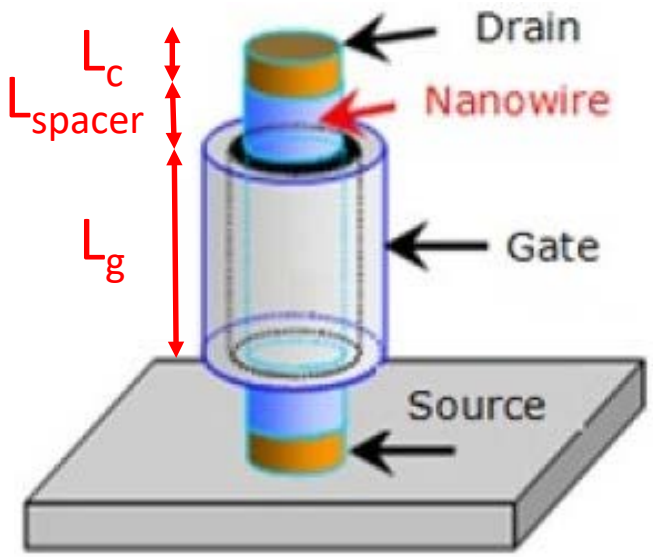




Vardi, EDL 2016

- First InGaAs FinFETs with W_f<10 nm
- Doubled g_m over earlier InGaAs FinFETs
- Short of Si FinFETs → sidewall quality?

Vertical nanowire MOSFET: ultimate scalable transistor



Vertical NW MOSFET:

→ uncouples footprint scaling from L_g, L_{spacer}, and L_c scaling

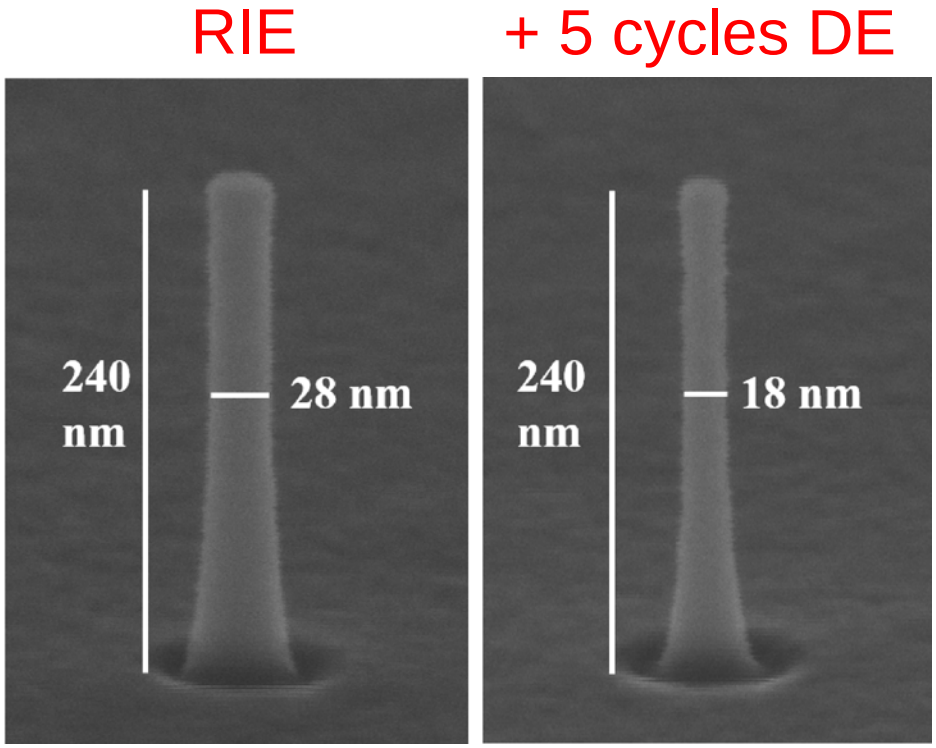
InGaAs Vertical Nanowires @ MIT

Key enabling technologies:

- RIE = $BCl_3/SiCl_4/Ar$ chemistry
- Digital Etch (DE) =

self-limiting O_2 plasma oxidation + H_2SO_4 or HCl oxide removal

- Radial etch rate=1 nm/cycle
- Sub-20 nm NW diameter
- Aspect ratio > 10
- Smooth sidewalls



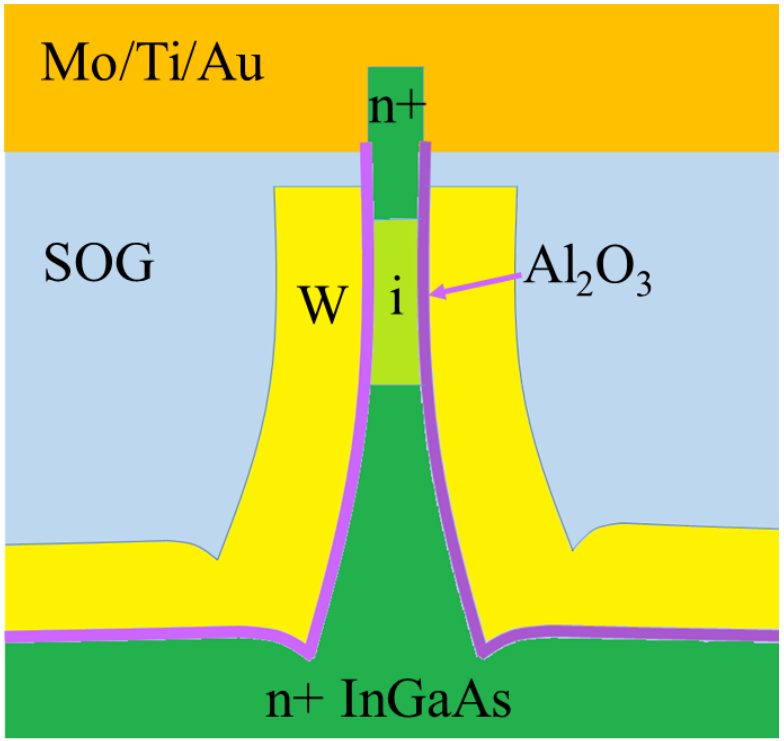
Zhao, IEDM 2013
Zhao, EDL 2014
Zhao, IEDM 2014

InGaAs VNW-MOSFETs by top-down approach @ MIT

Starting heterostructure:

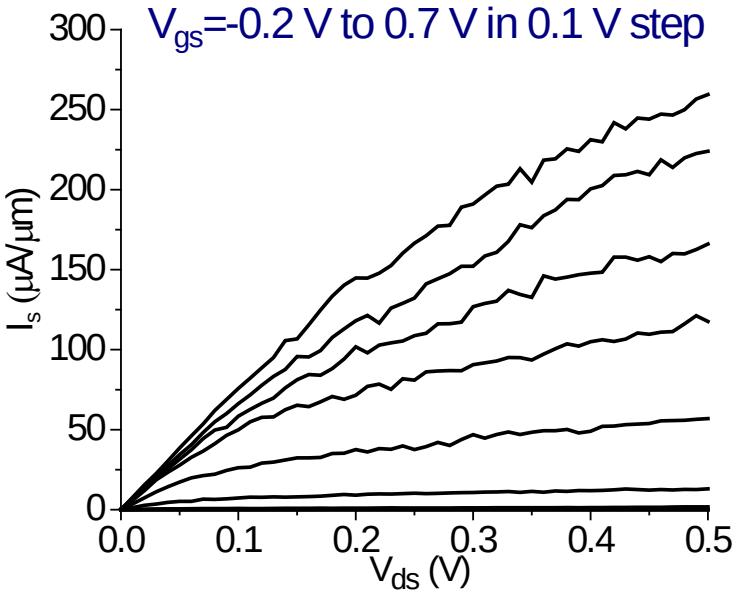
n^+ InGaAs, 70 nm
i InGaAs, 80 nm
n^+ InGaAs, 300 nm

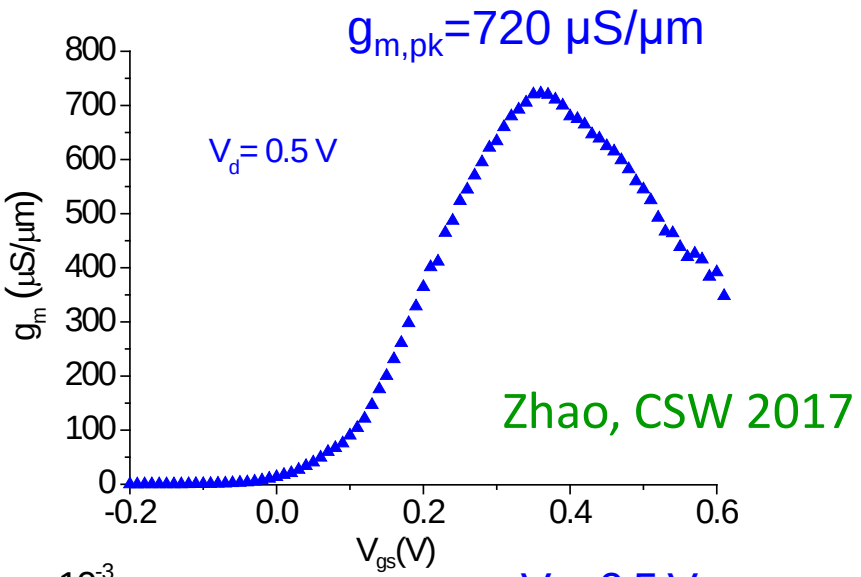
n^+: 6×10^{19} cm^{-3} Si doping

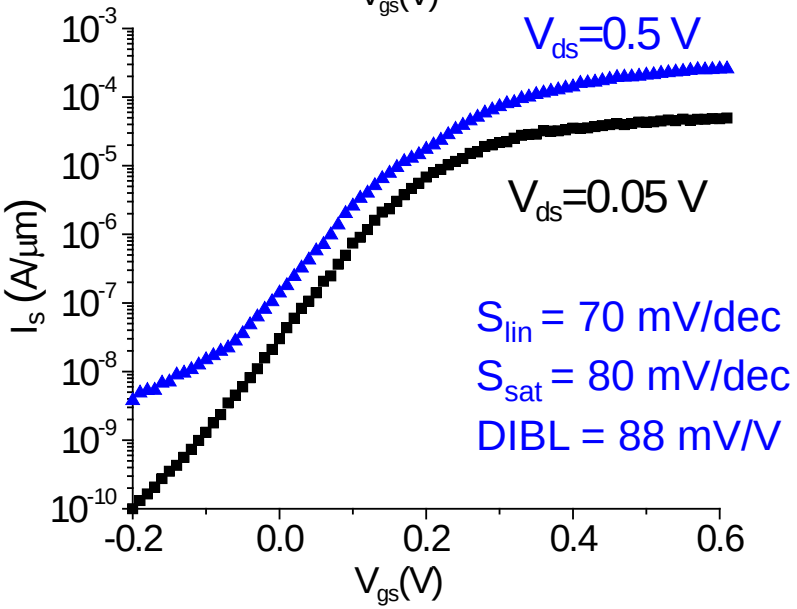


Top-down approach: flexible and manufacturable

NW-MOSFET I-V characteristics: D=40 nm





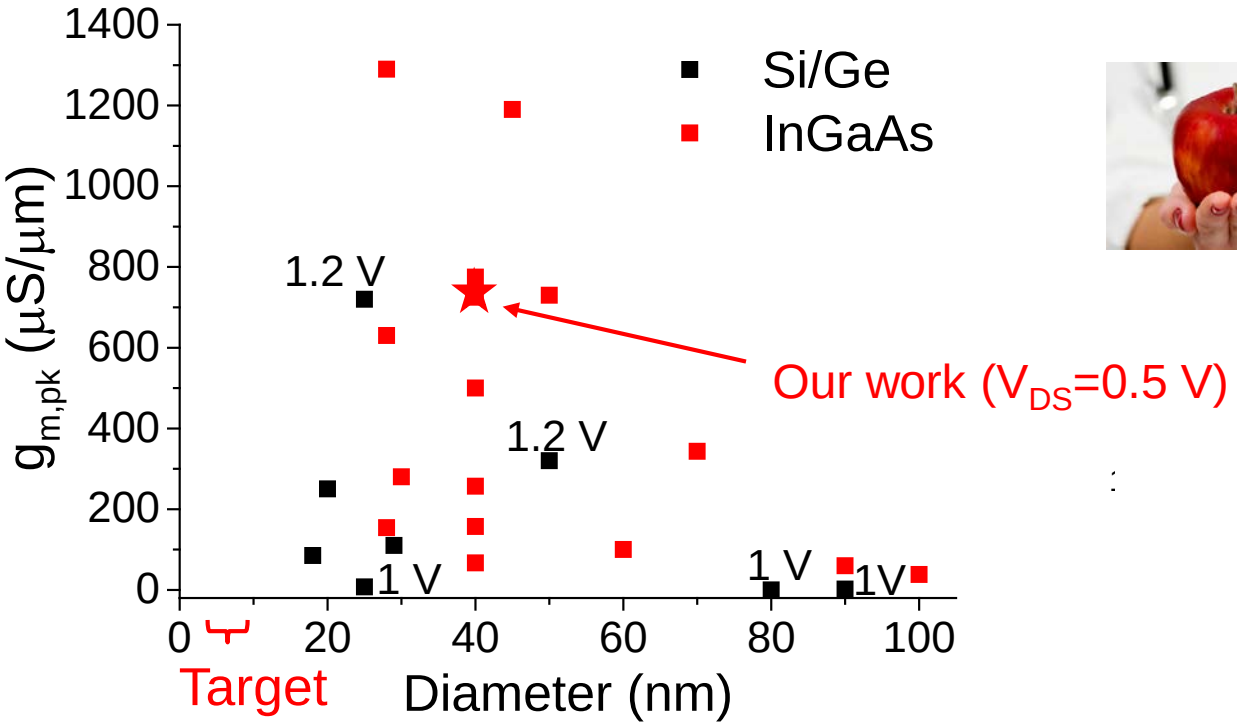


Single nanowire MOSFET:

- L_{ch}= 80 nm
- 3 nm Al_2O_3 (EOT = 1.5 nm)
- $g_{m,pk}$=720 μS/μm @ V_{DS}=0.5 V
- S_{lin}=70 mV/dec, S_{sat}=80 mV/dec
- DIBL=88 mV/V

Benchmark with Si / Ge VNW MOSFETs

Peak g_m of InGaAs (V_{DS}=0.5 V), Si and Ge VNW MOSFETs

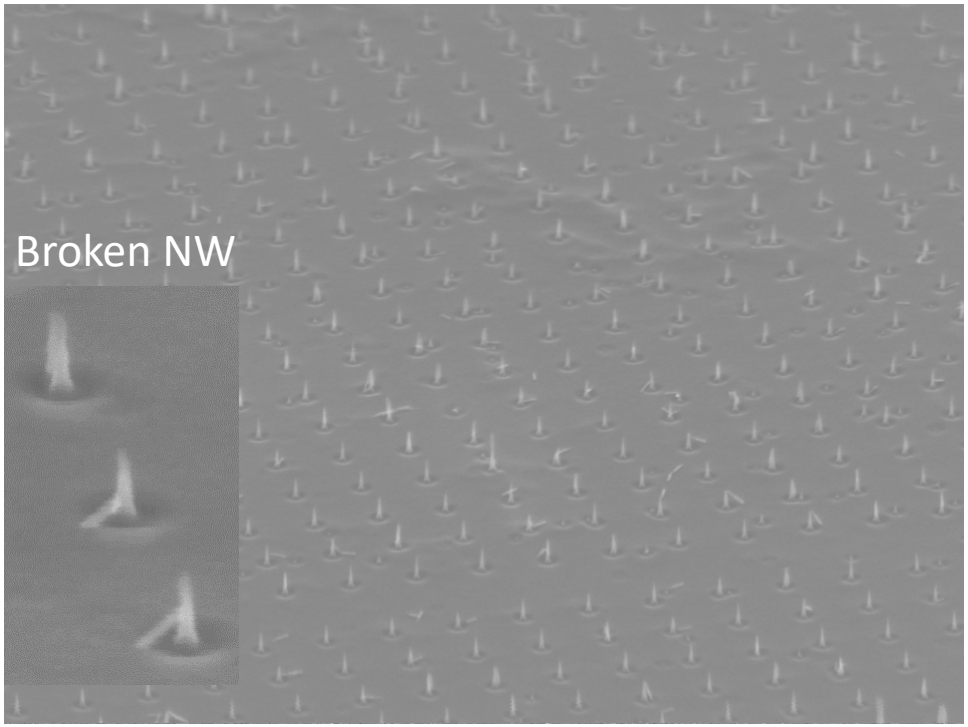


- InGaAs competitive with Si
- Need to demonstrate VNW MOSFETs with D<10 nm

InGaAs VNW Mechanical Stability for D<10 nm

8 nm InGaAs VNWs after 7 DE cycles:

8 nm InGaAs VNWs: Yield = 0%

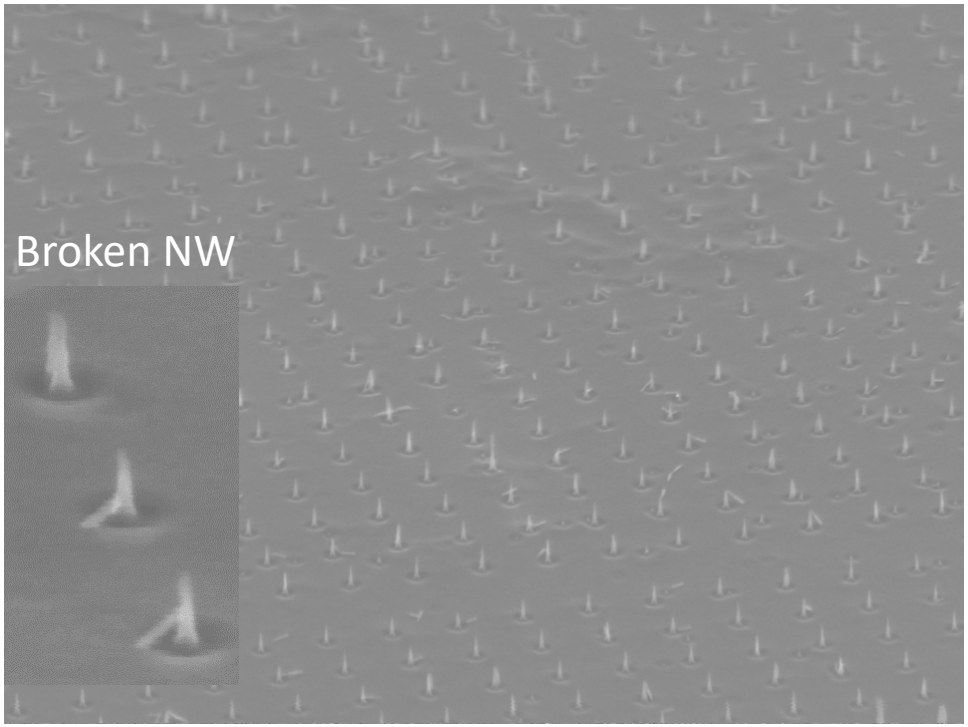


Difficult to reach 10 nm VNW diameter due to breakage

InGaAs VNW Mechanical Stability for D<10 nm

Difficult to reach 10 nm VNW diameter due to breakage

8 nm InGaAs VNWs: Yield = 0%



Water-based acid is problem:

Surface tension (mN/m):

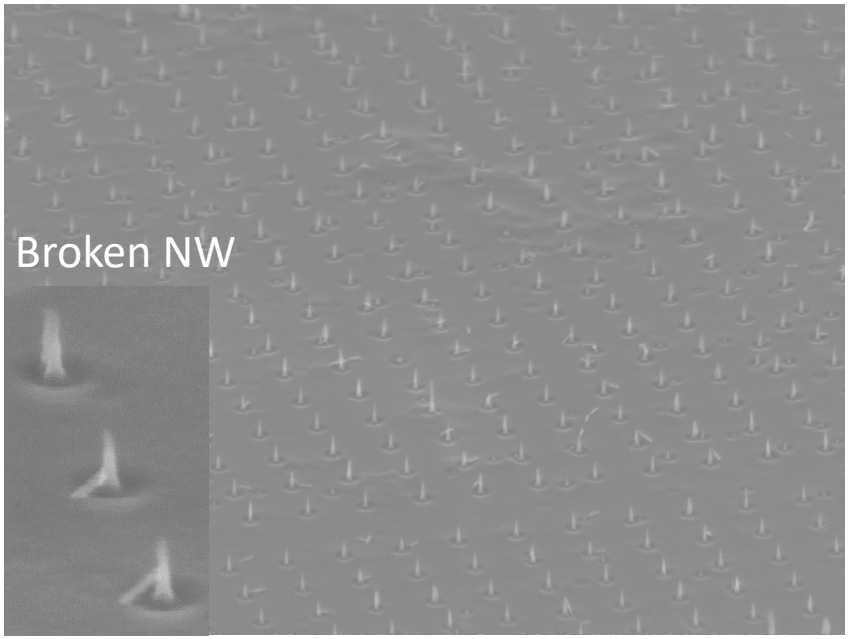
- Water: 72
- Methanol: 22
- IPA: 23

Solution: *alcohol-based digital etch*

Alcohol-Based Digital Etch

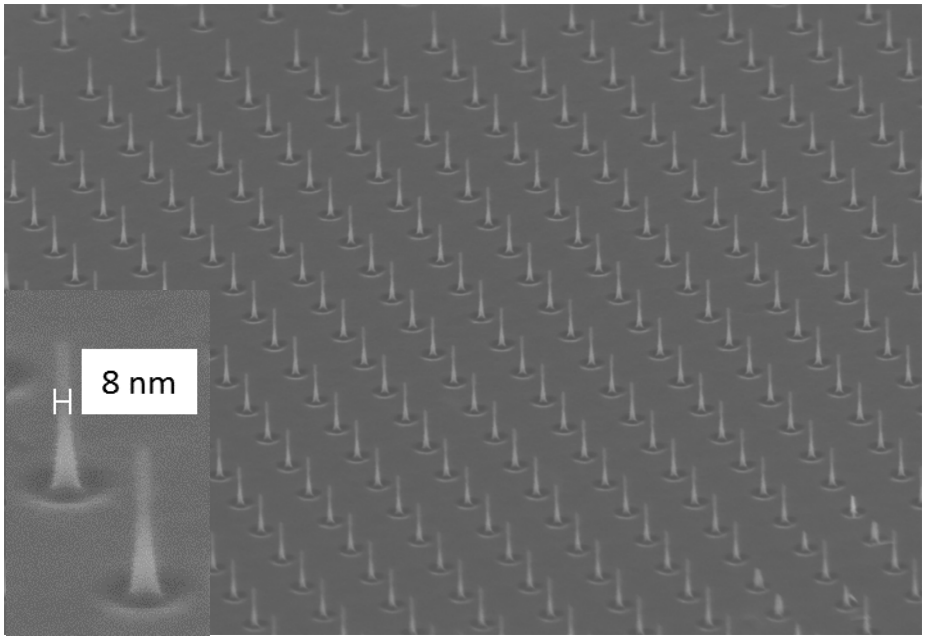
8 nm InGaAs VNWs after 7 DE cycles: Lu, EDL 2017

10% HCl in DI water
Yield = 0%



Radial etch rate: 1.0 nm/cycle

10% HCl in IPA
Yield = 97%

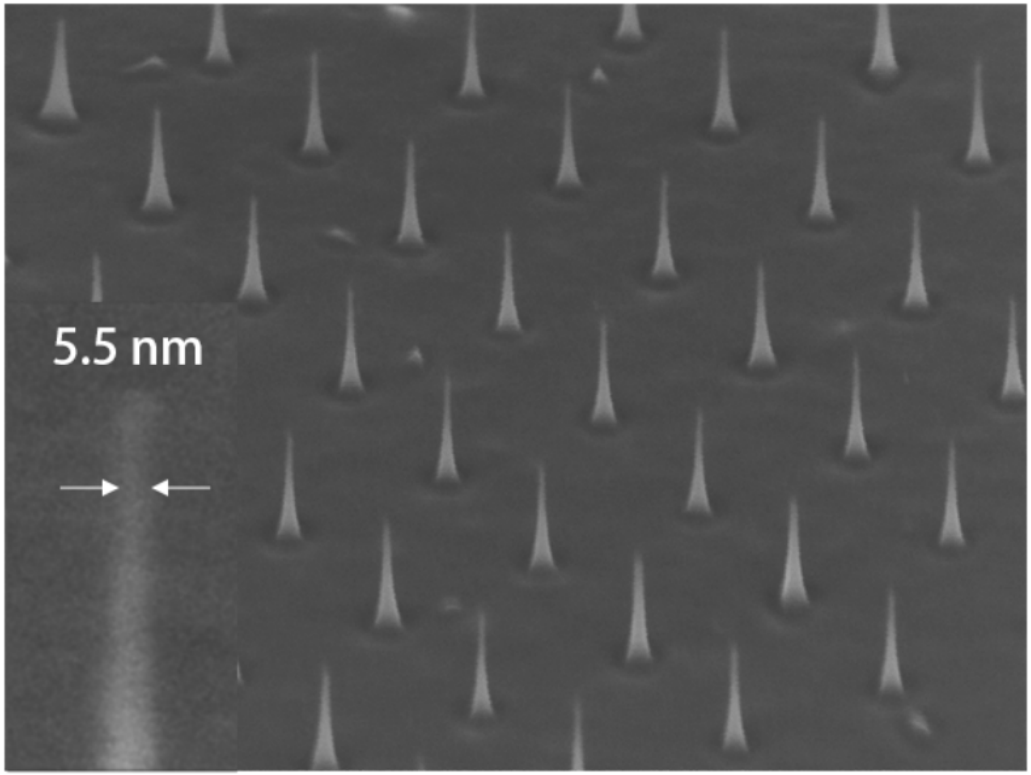


Radial etch rate: 1.0 nm/cycle

Alcohol-based DE enables D < 10 nm

D=5.5 nm VNW arrays

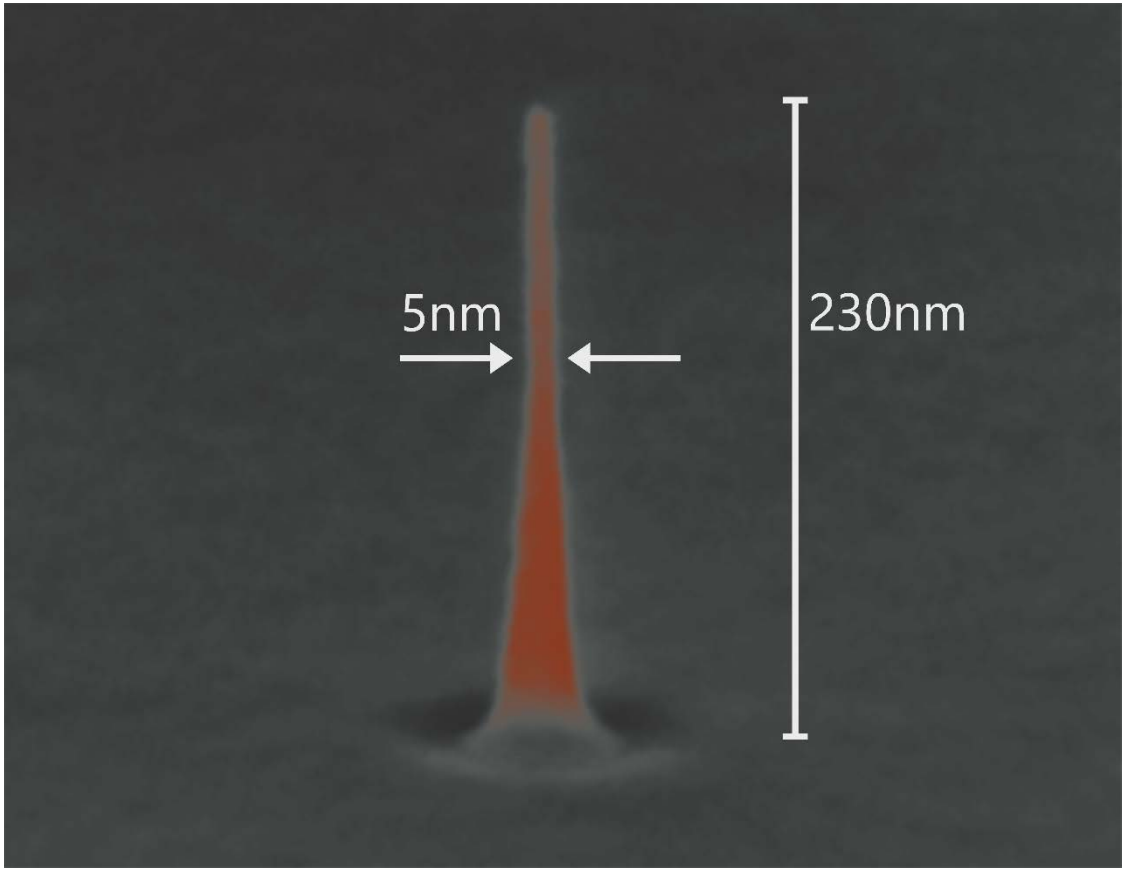
10% H_2SO_4 in methanol



90% yield

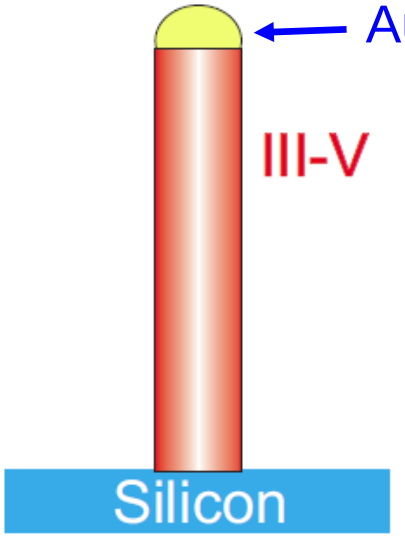
- H_2SO_4:methanol yields 90% at D=6 nm!
- Viscosity matters: methanol (0.54 cP) vs. IPA (2.0 cP)

InGaAs Digital Etch

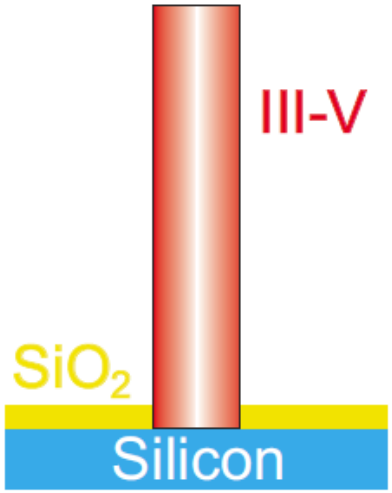


First demonstration of D=5 nm diameter InGaAs VNW
(Aspect Ratio > 40)

InGaAs Vertical Nanowires on Si by direct growth

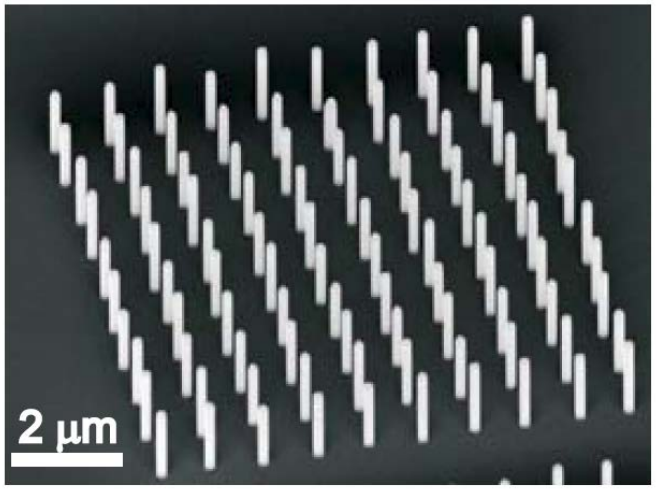


Vapor-Solid-Liquid (VLS) Technique

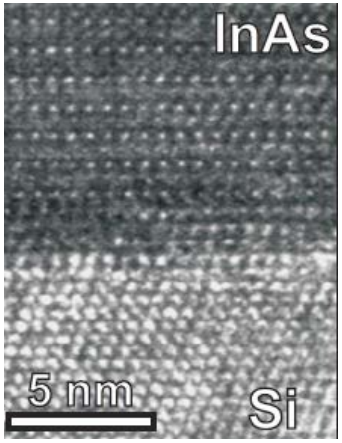


Selective-Area Epitaxy (SAE)

Riel, MRS Bull 2014



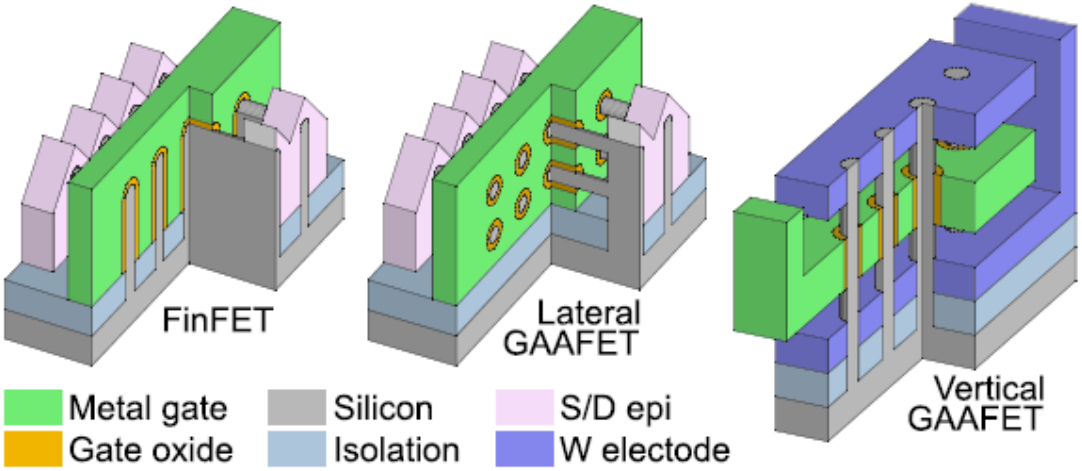
InAs NWs on Si by SAE

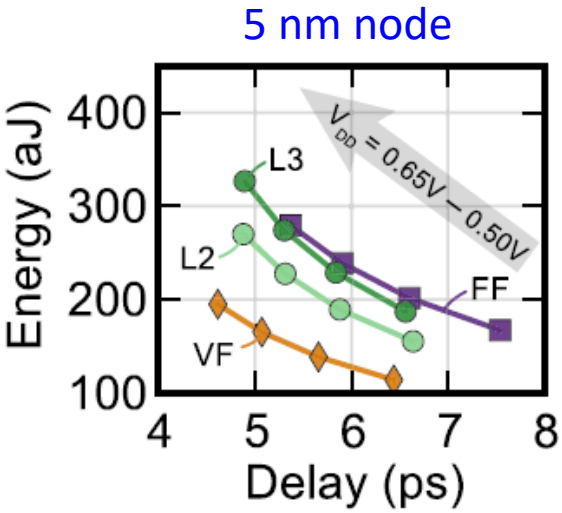


Riel, IEDM 2012

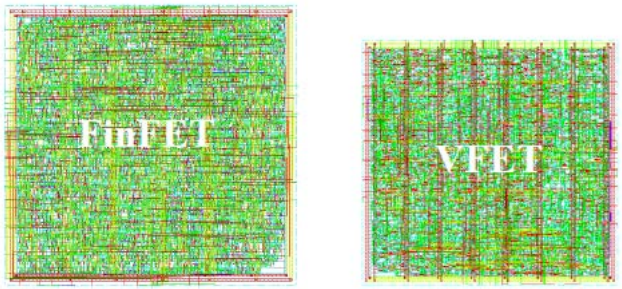
VNW MOSFETs: path for III-V integration on Si for future CMOS

Vertical nanowire MOSFET for 5 nm node





Yakimets, TED 2015
Bao, ESSDERC 2014



30% area reduction in 6T-SRAM
19% area reduction in 32 bit multiplier

Vertical NW:

→ power, performance and area gains w.r.t. Lateral NW or FinFET

Conclusions

1. Great recent progress on planar, fin and nanowire InGaAs MOSFETs
2. Device performance still lacking for 3D architecture designs
3. III-V Vertical-Nanowire MOSFETs: most likely architecture for future integration with Si
4. Many, MANY issues to work out:

sub-10 nm fin/nanowire fabrication, self-aligned contacts, device asymmetry, introduction of mechanical stress, V_T control, sidewall roughness, device variability, BTBT and parasitic HBT gain, oxide trapping, self-heating, reliability, NW survivability, co-integration on n- and p-channel devices on Si, interface states, metal routing, contact resistance < 10^{-9} $\Omega.cm^{-2}$, off-state leakage, TDDB, etc.…